36. The integrated circuit of claim 23 wherein the first silicon oxide layer is deposited on the substrate by placing the substrate in a process chamber and applying a sputtering power to reactants to generate a plasma in the process chamber, and wherein the second silicon oxide layer is deposited on the first silicon oxide layer by biasing the plasma toward the substrate while maintaining application of the sputtering power to the reactants.

REMARKS

Claims 16-36 are pending.

Claim 16

Claim 16 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onuki et al. To sustain a Section 102(b) rejection, the Examiner must establish that the reference discloses every element of the claim. In this case, **Onuki et al. does not disclose or suggest every element of claim 16.**

Onuki et al. discloses a switching bias sputtering process whereby d.c. sputtering and d.c. bias sputtering are operated alternately (page 182, right column, lines 9-11). As illustrated in Figs. 1 and 2, the switching bias sputtering process involves alternating step pulses of sputtering power and bias voltage. The step pulses of sputtering power and bias voltage alternate, and do not overlap in time. The use of the switching bias sputtering method is intended to enhance the step coverage and quality of Al films (page 182, right column, lines 12-13).

Onuki et al. does not disclose or suggest maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage.

The Examiner points to Fig. 1(a) in Onuki et al. for the disclosure of maintaining the application of the sputtering power while biasing the plasma toward the substrate. Applicants note that merely mentioning this conventional DC bias sputtering does not anticipate claim 16. Claim 16 recites depositing a first layer by sputtering without biasing

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the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma. Onuki et al. clearly does not teach depositing the two different layers. Nor does Onuki et al. recognize that the first layer formed without biasing the plasma is a reduced stress layer for reducing the stress of films deposited on the substrate (Page 4, lines 1-3 and Abstract). Therefore, claim 16 is novel and patentable over Onuki et al.

Claims 17-22 and 25-35

Claims 17, 18, 25-28, and 32-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., and Ramarotafika et al. Claims 19-22, 29-31, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. The Examiner recognizes that Ye et al. does not teach a controller or a memory storing a program for directing the operation of the system to deposit a first layer without biasing of the plasma and a second layer with biasing of the plasma. The Examiner relies on Onuki et al. for allegedly disclosing the deposition of a first layer without biasing and a second layer with biasing.

As discussed above, however, Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. Onuki et al. is devoid of any teaching or suggestion for depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

The remaining references do not cure the defects of Ye et al. and Onuki et al. The Examiner cites Boys et al. merely for allegedly disclosing a programmable memory controller for controlling a plasma deposition system. Ramarotafika et al. describes the influence of d.c. substrate bias on the resistivity, composition, crystallite size, and microstrain of WTi and WTi-N films. Matsuura discloses silicon oxide films in a semiconductor device allegedly having superior crack resistance, superior step coverage, and superior recess-filling characteristics (col. 3, lines 17-32 and Abstract). None of them teach or suggest depositing a first layer by sputtering without biasing the plasma and then depositing a second layer over the first layer by sputtering and biasing the plasma.

Moreover, Applicants contend that the rejection based on the combination of the references benefits from the exercise of hindsight. The references are directed to very different

processes for forming different films to achieve different purposes, as discussed in detail in the Preliminary Amendment filed on August 25, 2000.

Claims 23, 24, and 36

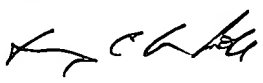
Claims 23, 24, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Applicants respectfully assert that these claims are patentable over the references because, for instance, the references do not teach or suggest an insulating layer formed between the metal layer and the semiconductor substrate and including a first silicon oxide layer and a second silicon oxide layer deposited using a high-density plasma chemical vapor deposition process, where the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer, as recited in claim 23 from which claims 24 and 36 depend.

Applicants respectfully assert that the Examiner has not established a *prima facie* case of obviousness, since the Examiner has not pointed to anything in the references that would suggest the claimed invention. Neither Onuki et al. nor Ramarotafika et al. teach depositing silicon oxide layers. Matsuura discloses silicon oxide layers, but fails to teach or suggest a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer. For at least the foregoing reasons, Applicants respectfully submit that claims 23, 24, and 36 are patentable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 650-326-2400.

Respectfully submitted,



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